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| Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION <i>(Use several sheets if necessary)</i> | Docket Number: 306812003501 | Application Number: Not Yet Assigned |
| | Applicant: Greg STARR | |
| | Filing Date: Concurrently Herewith | Group Art Unit: Not Yet Assigned |
| | Mailing Date: September 23, 2003 | |

U.S. PATENT DOCUMENTS

| Examiner Initials | Ref. No. | Date | Document No. | Name | Class | Subclass | Filing Date If Appropriate |
|-------------------|----------|------------|--------------|------------------|-------|----------|----------------------------|
| KL | 1. | 9/26/1995 | 5,453,706 | Yee | 326 | 93 | |
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| | 3. | 4/28/1998 | 5,744,991 | Jefferson et al. | 327 | 158 | |
| | 4. | 6/1/1999 | 5,909,126 | Cliff et al. | 326 | 41 | |
| | 5. | 4/4/2000 | 6,046,603 | New | 326 | 38 | |
| | 6. | 5/2/2000 | 6,057,704 | New et al. | 326 | 38 | |
| | 7. | 7/18/2000 | 6,091,263 | New et al. | 326 | 40 | |
| | 8. | 1/23/2001 | 6,177,844 B1 | Sung et al. | 331 | 25 | |
| | 9. | 1/30/2001 | 6,181,158 B1 | Cheung et al. | 326 | 38 | |
| | 10. | 4/10/2001 | 6,215,326 B1 | Jefferson et al. | 326 | 41 | |
| | 11. | 4/17/2001 | 6,218,876 B1 | Sung et al. | 327 | 156 | |
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FOREIGN PATENT DOCUMENTS

| Examiner Initials | Ref. No. | Date | Document No. | Country | Class | Subclass | Translation YES NO |
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(including author, title, date, pertinent pages, etc.)

| Examiner Initials | Ref. No. | Title |
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| KL | 13. | XILINX, XC4000E and XC4000X Series Field Programmable Gate Arrays, product information, 5/14/99, Version 1.6, 6-5 to 6-35. |
| AK | 14. | XILINX, Virtex™-E 1.8 V, Field Programmable Gate Arrays, product description, 7/23/01, 7 pgs. |

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| EXAMINER: LLM | DATE CONSIDERED: 3/31/04 |
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EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

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| <i>ku</i> | 15. | A. Mansukhani, "Phase Lock Loop Stability Analysis", Applied Microwave & Wireless, 2000, pp. 30-38. |
| <i>ku</i> | 16. | M. H. Perrott et al., "A 27-mW CMOS Fractional-N Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation", IEEE J. of Solid State Circuits, vol. 32, no. 12, Dec. 1997, 13 pgs. |
| <i>ku</i> | 17. | Altera, "Phase-Locked Loop (PLL) and LVDS Support in APEX 20KE Devices", Marketing Bulletin #276, 1/2000, 3 pgs. |
| <i>ku</i> | 18. | Texas Instruments, "Low-Voltage 1.2 GHz Fractional-N/Integer-N Synthesizer", TRF 2050, 34 pgs., 6/96 revised 10/2000. |
| <i>ku</i> | 19. | B. Hazavi, RF Microelectronics, "RF Synthesizer Architectures", 1998, pp. 270-280. |

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| EXAMINER: <i>LUU</i> | DATE CONSIDERED: <i>3/31/04</i> |
| EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant. | |